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CHAPTER 67

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INTEGRATED CIRCUITS

Jack Kilby would justly be considered one of the greatest electrical engineers of all time for one invention; the monolithic integrated circuit, or microchip. He went on to develop the first industrial, commercial and military applications for this integrated circuits- including the first pocket calculator (pocketronic) and computer that used them

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67.1. Introduction

Electronic circuitry has undergone tremendous changes since the invention of a triode by Lee De Forest in 1907. In those days, the active components (like triode) and passive components (like resistors, inductors and capacitors etc.) of the circuits were **separate and distinct units** connected by soldered leads.

With the invention of the transistor in 1948 by W.H. Brattain and I. Bardeen, the electronic circuits became considerably reduced in size. It was due to the fact that a transistor was not only cheaper, more reliable and less power consuming but was also much smaller in size than an electron tube. To take advantage of small transistor size, the passive components too were greatly reduced in size thereby making ***the entire circuit very small.*** Development of printed circuit boards (*PCBs*) further reduced the size of electronic equipment by eliminating bulky wiring and tie points.

In the early 1960s, a new field of **microelectronics** was born primarily to meet the requirements of the Military which wanted to reduce the size of its electronic equipment to approximately one-tenth of its then existing volume. This drive for extreme reduction in the size of electronic circuits has led to the development of microelectronic circuits called **integrated circuits (ICs)** which are so small that their actual construction is done by technicians using high powered microscopes.

67.2. What is an Integrated Circuit ?

To put it very briefly, an integrated circuit (*IC*) is **just a packaged electronic circuit.**

A more detailed definition is as under :

An *IC* is a complete electronic circuit in which both the active and passive components are fabricated on a tiny single chip of silicon.

Active components are those which have the ability to produce gain. Examples are : transistors and *FETs*.

Passive components or devices are those which do not have this ability. Examples are : resistors, capacitors and inductors.

ICs are produced by the same processes as are used for manufacturing individual transistors and diodes etc. In such circuits, different components are isolated from each other by isolation diffusion within the crystal chip and are interconnected by an aluminium layer that serves as wires.

A discrete circuit, on the other hand, is one ***that is built by connecting separate components.*** In this case, each component is produced separately and then all are assembled together to make the electronic circuit.

J.S. Kilby of Texas Instruments was the first person to develop (in 1959) an integrated circuit — a single monolithic silicon chip in which active and passive components were fabricated by successive deposition, etching and diffusions. He was soon followed by Robert Noyce of Fairchild who successfully fabricated a complete *IC* including the interconnections on a single silicon chip. Since then the evolution of this technology is fast-paced.

67.3. Advantages of ICs

As compared to **standard printed circuits** which use discrete components, *ICs* have the following advantages :

1. Extremely small physical size

Often the size is thousands of times smaller than a discrete circuit. The various components and their interconnections are distinguishable only under a powerful microscope.

2. Very small weight

Since many circuit functions can be packed into a small space, complex electronic equipment can be employed in many applications where weight and space are critical, such as in aircraft or space-vehicles.

3. Reduced cost

It is a major advantage of *ICs*. The reduction in cost per unit is due to the fact that many identical circuits can be built simultaneously on a single wafer—this process is called **batch fabrication.** Although the processing steps for the wafer are complex and expensive, the large number of resulting integrated circuits make the ultimate cost of each *IC* fairly low.

4. Extremely high reliability

It is perhaps the **most important** advantage of an *IC* and is due to many factors. Most significant factor is the absence of soldered connections. Another is the need for fewer interconnections—the major cause of circuit failures. Small temperature rise due to low power consumptions of *ICs* also improves their reliability. In fact, an *IC* logic gate has been found to be 100,000 times more reliable than a vacuum tube logic gate and 100 times more reliable than a transistor logic gate.

Obviously, higher reliability means that *ICs* will work for longer periods without giving any trouble—something most desirable from both military and consumer application point of view.

5. Increased response time and speed

Since various components of an *IC* are located close to each other ***in*** or ***on*** a silicon wafer, the time delay of signals is reduced. Moreover, because of the short distances, the chance of stray electrical pickup (called parasitic capacitance) is practically nil. Hence it makes them very suitable for small signal operation and high frequency operation. As a result, the response time or the operating speed of the system is improved.

6. Low power consumption

Because of their small size, *ICs* are more suitable for low power operation than bulky discrete circuits.

7. Easy replacement

ICs are hardly ever repaired because in case of failure, it is more economical to replace them than to repair them.

8. Higher yield

The ***yield*** is the percentage of usable devices. Because of the batch fabrication, the yield is very high. Faulty devices usually occur because of some defect in the silicon wafer or in the fabrication steps. Defects in silicon wafer can occur because of lattice imperfection and strains introduced in crystal growth, cutting and handling of the wafers. Usually such defects are extremely small, but their presence can ruin devices built on or around. Reducing the size of each device greatly increases the chance for a given device to be free of such defects. The same is true for fabrication defects such as the presence of a dust particle on the photolithographic mask.

67.4. Drawbacks of ICs

The integrated circuits suffer from the following drawbacks :

1. coils or inductors cannot be fabricated,
2. *ICs* function at fairly low voltages,
3. they handle only limited amount of power,
4. they are quite delicate and cannot withstand rough handling or excessive heat.

However, the advantages of *ICs* far outweigh their disadvantages or drawbacks.

67.5. Scale of Integration

Level of integration in *ICs* has been increasing ever since they were developed some three and a half decades back. The number of electronic circuits or components that can be fitted into a standard size *IC* has been dramatically increasing with each passing year. In fact, whole **electronic systems** rather than just **a circuit** are incorporated in one package.

An approximate method of classifying the amount of circuit or component density is as follows:

1. SSI—*small scale integration*

In this case, the number of **circuits** contained in one *IC* package is less than 12 (or number of **components** is less than 50).

2. MSI—*medium scale integration*

Here, number of circuits per package is between 13 and 99 (or number of components is between 50 and 5000).

3. LSI—*large scale integration*

In this case, circuit density is between 100 and 9,999 (or component density is between 5000 and 100,000).

4. VLSI—*very large scale integration*

Here the number of circuits per package is between 10,000 to 99,999 (or number of components is between 100,000 – 1,000,000).

5. ULSI—*ultra large scale integration*

In this case, the circuit density is between 100,000 to 999,999 (or component density is between 1,000,000 – 10,000,000).

6. GSI—*Giga scale integration*

Here the number of circuits per package is 1,000,000 or more (or number of components are over 100,000,000).

In summary,

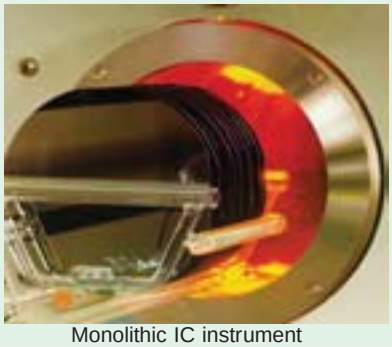
SSI	<	12	circuits per chip
MSI		12 – 99	
LSI		100 – 9,999	
VLSI		10,000 – 99,999	
ULSI		100,000 – 999,999	
GSI	>	1,000,000	

67.6. Classification of ICs by Structure

Structurally speaking, *ICs* can be classified into the following three types :

1. Monolithic Integrated Circuits

The word 'monolithic' means 'single stone' or more appropriately 'a single-solid structure'. In this *IC*, all circuit components (both active and passive) are fabricated inseparably within a single continuous piece of silicon crystalline material called **wafer (or substrate).** All components are **atomically** part of the same chip. Transistors, diodes and other passive components are fabricated at appropriate spots in the substrate using epitaxial diffusion technique.


Monolithic IC instrument

Component interconnections are provided on the surface of the structure and external connecting wires are taken out to

the terminals. It is a complete circuit requiring no 'add ons'.

Despite some of its distinct disadvantages, monolithic *ICs* are in wide use because for mass production, monolithic process has been found to be the most economical.

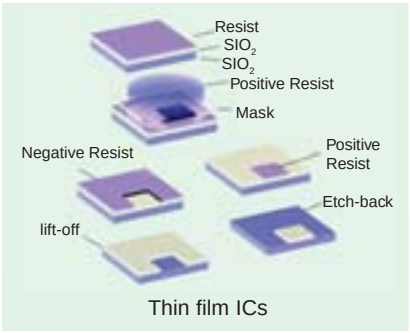
2. Thick and Thin-Film ICs

The essential difference between thick-film and thin-film *ICs* *is not their relative thickness but* the **method** of depositing the film. Both have similar appearance, properties and general characteristics though they both differ in many respects from monolithic *ICs.* These *ICs* are not formed **within** a silicon wafer but **on** the surface of an insulating substrate such as glass or a ceramic material. Moreover, **only passive components** (resistors, capacitors) are formed through thick or thin-film techniques on the insulating surface. The active elements (transistors, diodes) are added externally as **discrete elements** to complete a functional circuit. These discrete active components are frequently produced by using the monolithic process.

As stated above, the primary difference between the thick and thin film techniques is the process used for forming passive components and the metallic conduction pattern.

(*a*) Thin-film ICs

Such circuits are constructed by depositing films (typically 0.1 to 0.5 μm) of conducting material through a mask on the surface of a substrate made of glass or ceramic. Resistors and conductors are formed by varying the width and thickness of the film and by using materials of different resistivity. Capacitors are produced by sandwiching an insulating oxide film between two conducting films. Small inductors can be made by depositing a spiral formation of film. The active components like transistors and diodes etc. are externally added and inter-connected by wire bonds.



Thin film ICs

Following two methods are used to produce thin films :

(*i*) vacuum evaporation

In this method, the vaporised material is deposited through a set of masks on the glass or ceramic substrate contained in vacuum.

(*ii*) cathode sputtering

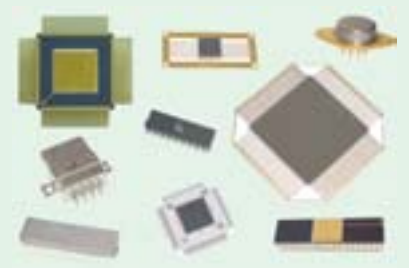
In this method, atoms from a cathode made of the desired film material are deposited on the substrate which is located between the cathode and the anode.

(*b*) Thick-film ICs

Such type of integrated circuits are sometimes referred to as **printed** thin-film circuits. They are so called because silk-screen printing techniques are employed to create the desired circuit pattern on the surface of the substrate. The screens are made of fine stainless steel wire mesh and the 'inks' are pastes (of pulverised glass and aluminium) which have conductive, resistive or dielectric properties. After printing, the circuits are high-temperature fired in a furnace to fuse the films to the insulating substrate. As with thin-film *ICs*, active elements are added externally as discrete components.

3. Hybrid or Multichip ICs

As the name implies, such circuits are formed either by inter-connecting a number of individual chips or by a combination of film and monolithic *IC* techniques. In such *ICs*, active components are first formed within a silicon wafer (using monolithic technique) which is subsequently covered with an insulating layer such as SiO_2. Film techniques are then employed to form passive components on the SiO_2 surface. Connections are made from the film to the monolithic structure through 'windows' cut in the SiO_2 layer.


Hybrid or Multichip ICs

67.7. Comparison Between Different ICs

Each type of *IC* has its own advantages and disadvantages.

Monolithic circuits have ***the advantage of lowest cost and highest reliability.*** However they have the following disadvantages :

1. isolation between components is poorer,
2. range of values of passive components used in the circuits is comparatively small,
3. inductors cannot be fabricated,
4. they afford no flexibility in circuit design because for making any changes in the circuit, **a new set of masks is required.**

The film circuits have the advantage of forming passive components with broader range of values and reduced tolerances as compared to monolithic circuits. Isolation between their components is also better since they are deposited on a substrate that is an insulator. Use of external discrete active components allows greater flexibility in circuit design. These circuits also give better high frequency performance than monolithic circuits.

However, they suffer from the disadvantages of

1. not being able to fabricate active components,
2. comparatively higher cost and 3. larger physical size.

The chief advantage of multichip *ICs* is their greater flexibility but they are **too expensive** for mass production and **have least reliability.** Hence, such circuits are generally used as prototypes for monolithic *ICs*.

The various integrated circuits are arranged in the form of an '*IC*' tree of Fig. 67.1.

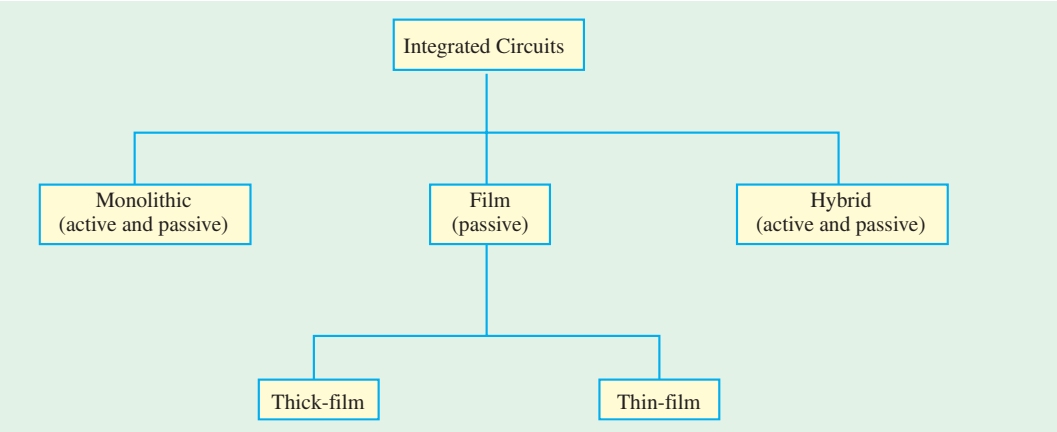


Fig. 67.1

67.8. Classification of ICs By Function

The earlier classification of ICs was based on ***their method of construction.*** However, the integrated circuits can also be classified according to their general function. The two most important categories are :

1. linear and 2. digital

The same fact has been shown in Fig. 67.2.

Examples of linear *ICs* are :

1. *BEL CA*-3020—used as multipurpose wide-band power amplifier.

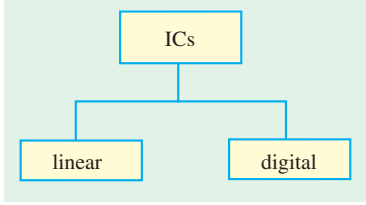


Fig. 67.2

2. *BEL CA*-3065—it is a monolithic *IC* which combines a multistage *IF* amplifier, limiter, an *FM* detector, an electronic attenuator, a Zener diode regulated power supply and an audio amplifier. In fact, this *IC* provides a high performance multistage sub-system of a TV receiver. It is available in 14-pin dual-in-line package.

Both are manufactured by Bharat Electronics Ltd., Bangalore.

3. SSD 710—is a linear *IC* used as Differential Comparator

It is manufactured by Solid State Devices, Syed Abdullah Road, Bombay.

An example of a digital *IC* is

1. *BEL* 7400—is a *TTL* IC gate which provides designer with one of the gating logic necessary to design medium-speed digital control and data processing systems. It is available in 14-pin dual-in-line plastic package.

67.9. Linear Integrated Circuits (LICs)

LICs are also referred to as analog *ICs* because their inputs and outputs can take on a continuous range of values and the outputs are generally proportional to the inputs. As compared to digital *ICs*, *LICs* are used much less. But *LICs* are quickly displacing their discrete circuit counterparts in many applications as their cost becomes competitive. They also possess much higher reliability because so many external connections (major source of circuit failure) are eliminated. *LICs* find wide use in military and industrial applications as well as in consumer products. They are frequently used in

Linear ICs

1. operational amplifiers,
2. small-signal amplifiers,
3. power amplifiers,
4. *RF* and *IF* amplifiers,
5. microwave amplifiers,
6. multipliers,
7. voltage comparators,
8. voltage regulators etc.

Operational amplifier is by far the most versatile form for an *LIC* and is discussed separately.

67.10. Manufacturer's Designation of LICs

Each manufacturer assigns a specific code and type number to the *LICs* produced by him. For example, an internally-compensated op-amp 741 produced by Fairchild is designated as µA 741. Here, µA is the identifying code used by Fairchild. Many other manufacturers produce *LICs* similar to 741 but use their own code while retaining the same type number. For example, Fiarchild's original µA 741 is manufactured by other manufacturers with the following codes :

1. National Semiconductor —— *LM* 741
2. Motorola —— *MC* 1741
3. RCA —— *CA* 3741
4. Texas Instruments —— *SN* 5274

It is seen that the last three digits in each manufacturer's designation are the same *i.e.* 741. All these op-amps have the same specifications. Hence, in practice, the manufacturer's code number is often ignored and all such *LICs* are referred to as 741.

Many *LICs* are available in different classes such as A, B, C, E, S and SC. For example, main classes of 741 are as under :

741	——	Military grade op-amp
741 C	——	Commercial grade op-amp
741 A	——	Improved version of 741
741 E	——	Improved version of 741 C
741 S	——	Military grade op-amp with higher slew rate
741 SE	——	Commercial grade op-amp with higher slew rate

67.11. Digital Integrated Circuits

About 80 per cent of the *IC* market has been captured by digital *ICs* which are mostly utilized by the computer industry. Digital *ICs* lend themselves easily to monolithic integration because a computer ***uses a large number of identical circuits.*** Moreover, such circuits employ relatively few capacitors and values of resistances, voltages and currents are low.

Digital *ICs* contain circuits whose input and output voltages are limited to **two** possible levels—low or high. It is so because ***digital signals are usually binary.*** Sometimes, digital circuits are referred to as switching circuits. Digital *ICs* include circuits such as

1. logic gates **2.** flip-flops **3.** counters **4.** clock-chips
5. calculator chips **6.** memory chips **7.** microprocessors (μP) etc.

67.12. IC Terminology

Some of the common terms used in fabricating integrated circuits are defined below :

1. **Bonding** – attaching the die on the ceramic substrate and then connecting the leads to the package.
2. **Chip** – an extremely small part of a silicon wafer on which *IC* is fabricated. A photograph of the wafer containing hundreds of chips (or dice) and a drawing of a chip are shown in Fig. 67.3. The identical chips, each of which may vary in area from 10 to over 100 mm^2, may contain up to several million devices.

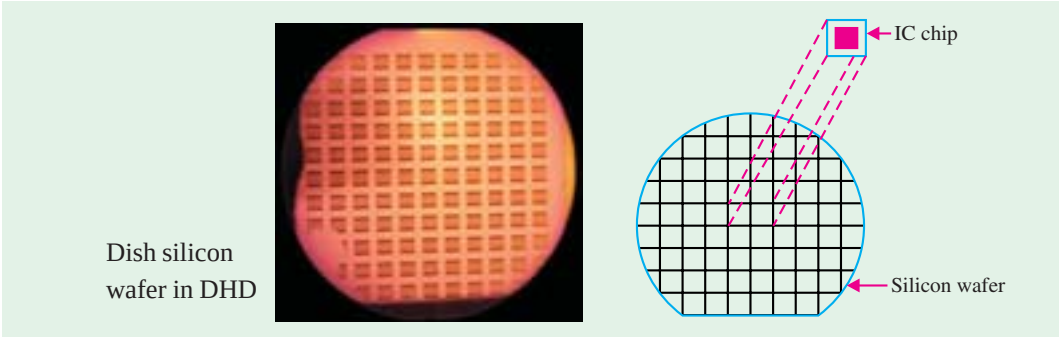


Fig. 67.3

3. **Circuit probing** – testing the electrical performance of each *IC* chip with the help of a microscope and multi-point probe.
4. **Die** – same as a chip.
5. **Diffusion** – a process that consists of the introduction of impurities into selected regions of a wafer to form junctions.
6. **Encapsulation** – putting a cap over the *IC* and sealing it in an inert atmosphere.

7. **Epitaxy** – a process of the controlled growth of a crystalline doped layer of silicon on a single crystal substrate.
8. **Etching** – a process of selective removal of regions of a semiconductor, metal or silicon dioxide.
9. **Mask** – a glass plate with desired pattern for diffusion or metallization. Usually a single mask is not sufficient to fabricate an *IC*.
10. **Metallization** – a process for providing ohmic contacts and interconnections by evaporating aluminium over the chip.
11. **Photolithography** – a process to transfer geometrical pattern from the mask to the surface of the wafer.
12. **Photoresist** – a light-sensitive material that hardens when exposed to ultraviolet light.
13. **Wafer** – a thin disk of semiconductor in which number of *ICs* are fabricated simultaneously.

67.13. Semiconductors Used in Fabrication of ICs and Devices

The fabrication of *ICs* has been based on the use of silicon (Si) as the premier semiconductor. Two other semiconductors used for *IC* fabrication are germanium and gallium arsenide (GaAs). But these semiconductors present special problems for device fabrication as discussed below.

Gallium arsenide has very attractive electrical properties but its crystals have a high density of defects which limit the performance of devices made from it. Moreover gallium arsenide is more difficult to grow in single crystal form. Both silicon and germanium do not suffer from these problems. On the plus side, gallium arsenide has an electron velocity that is larger than silicon. Because of this gallium arsenide devices are faster than silicon devices. Also, gallium arsenide has a lower saturation electric field than silicon. Because of this, the gallium arsenide devices have lower power-delay product. Devices made from substrates of gallium arsenide have lower parasitic capacitances. This property contributes to their speed advantage over the silicon devices. Another advantage of gallium arsenide results from direct band gap which makes it possible to provide certain functions not possible in silicon such as ***coherent* and *incoherent light emission.***

A major advantage of silicon, in addition to its abundant availability in the form of sand, is that it is possible to form a superior stable oxide (SiO_2). This oxide has superb insulating properties and provides an essential and excellent ingredient in the fabrication and protection of devices or *ICs*. On the other hand, germanium oxide is unsuited for device applications. The intrinsic resistivity of germanium is 47 Ω-cm, while that of silicon is 230,000 Ω-cm. The low resistivity of germanium would have precluded the fabrication of rectifying devices with high breakdown voltages. Thus high-voltage rectifying devices and certain infrared sensing devices are practical with silicon. Finally, there is an economic consideration and that is electronic grade germanium is now more costly than silicon. Thus, at present time, silicon remains the major semiconductor in the fabrication of *ICs*.

Some other semiconductors used in semiconductor industry are gallium phosphide (GaP), gallium nitride (GaN), zinc sulphide (ZnS), indium antimonide (InSb), compound of cadmium and selenium (CdSe). GaAs, GaP and GaN are used in high-speed devices and devices requiring emission and absorption of light such as lasers and light emitting diodes (LEDs). ZnS is used as fluorescent material such as those in television screens. In Sb and CdSe are used as light detectors.

67.14. How ICs are Made ?

The *ICs* are manufactured in four distinct stages (refer to Fig. 67.4). These are **(1)** material preparation, **(2)** crystal growing and wafer preparation, **(3)** wafer fabrication and **(4)** testing, bonding and packaging. All these stages are discussed one by one in the following pages.

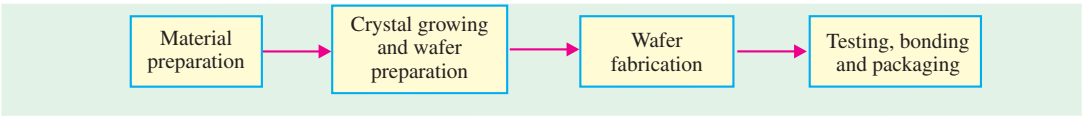


Fig. 67.4

67.15. Material Preparation

Silicon, as an element is not found in nature. However, it is found abundantly in nature in the form of silicon dioxide, which constitutes about 20% of earth's crust. Silicon is commonly found as quartz or sand. A number of processes are required to convert sand into pure silicon with a polycrystalline structure. Fig. 67.5 shows the different processes involved in the preparation of polycrystalline silicon from sand. As seen from this figure, the sand is allowed to react with a gas produced from the burning of carbon (coal, coke and wood chips). This produces silicon with 98% purity. Next silicon is further purified in a reactor to produce electronic-grade polycrystalline silicon.

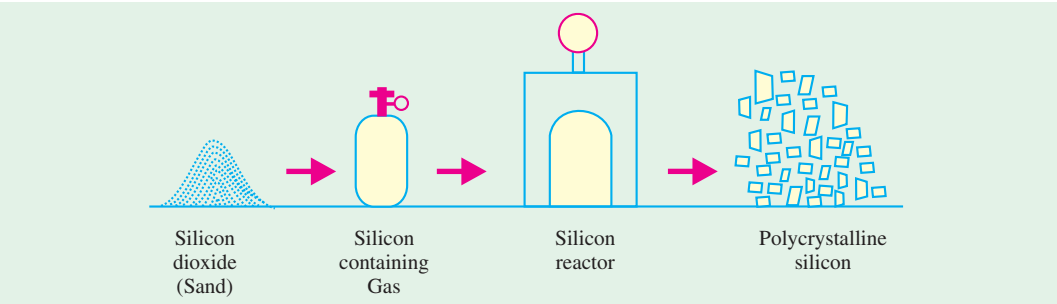


Fig. 67.5

67.16. Crystal Growing and Wafer Preparation

The polycrystalline silicon is composed of many small crystals having random orientation and containing many defects. For silicon to be used in the fabrication of *ICs*, it must be nearly perfect and crystalline in nature. We, therefore, now need to produce single crystals of silicon. This is done by a process called crystal growth. There are two methods to carryout the crystal growth : (***i***) the ***Czochralski*** and (*ii*) the ***flat zone*** process. The Czochralski process prepares virtually all the silicon used for *IC* fabrication. The flat zone process is used to prepare crystals for fabricating high-power, high voltage semiconductor devices.

The Czochralski process. The equipment used for single crystal growth (called puller) is as shown in Fig. 67.6. The puller has three main components : **(*i*)** a furnace which includes quartz crucible, a rotation mechanism (clockwise as shown), and a radio frequency (*RF*) heating element, **(*ii*)** a crystal pulling mechanism which includes a seed holder and a rotation mechanism (counter-clockwise), and **(*iii*)** an ambient control which includes an argon gas source, a flow control and an exhaust system. In addition the puller has a computer system to control process parameters such as temperature, crystal diameter, pull rate and rotation speed.

To grow crystals, the polycrystalline silicon is placed in the crucible. The furnace is heated to a temperature of 1690 K which is slightly greater than the melting point (1685 K) of silicon. A precisely controlled amount of dopant (boron or phosphorus) is added to the melt to make the silicon as *P*-type or *N*-type. A suitable oriented seed crystal (*i.e.*, a small highly perfect crystal) is suspended over the crucible in a seed holder. The seed is inserted into the melt and a small portion of it is

allowed to melt. The seet is rotated and pulled up very slowly, while at the same time, the crucible is rotated in the opposite direction. The molten silicon attaches itself to the seed and it becomes identical to the seed in structure and orientation. As the seed is pulled up, the material that is attached to the seed solidifies (*i.e.*, freezes). Its crystal structure becomes the same as that of the seed and a larger crystal is formed. Thus using this method, cylindrical single crystal bars (called ingots) of silicon are produced.

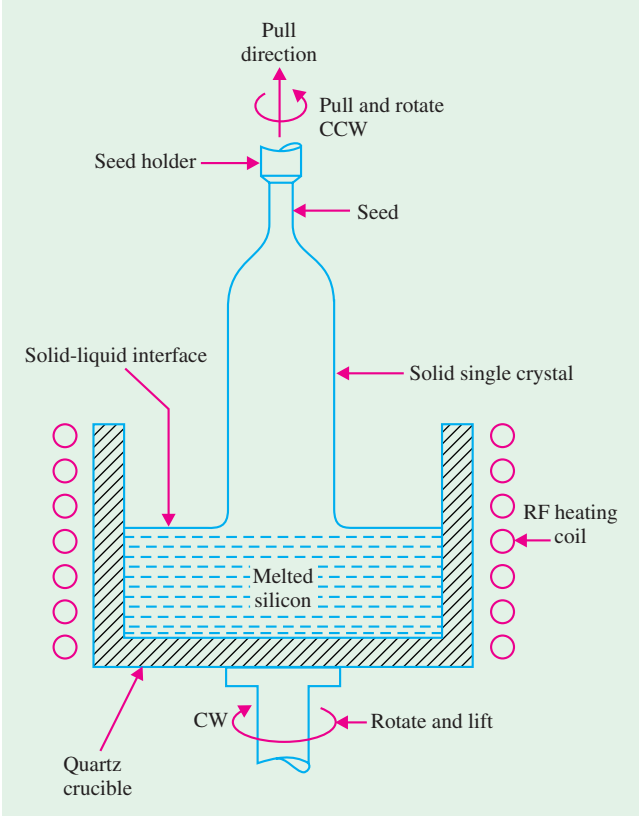


Fig. 67.6

The desired diameter of the silicon ingot is obtained by controlling both the temperature and the pulling speed. In the final step, when the bulk of the melt has been grown, the crystal diameter is decreased until there is a point contact with the melt. The resulting ingot is cooled and is removed to be made into thin discs called ***wafers***. The ingots have diameters as large as 200 mm with the latest ones approaching 300 mm. The ingot length is of the order of 1000 mm.

Wafer preparation : In this stage the ingot surface is grounded throughout to an exact diameter and the top and bottom portions are cut off. After that one or more flat regions are ground along the length of the ingot. These flat regions mark the specific crystal orientation of the ingot and conductivity type (*i.e.*, *P*-type or *N*-type) of silicon material. Refer to Fig. 67.7.

Notice that the ingot is marked with two flats regions : ***(i)*** the larger flat (called primary flat) and ***(ii)*** the smaller flat or secondary flat regions. The primary flat allows a mechanical locator in automatic processing equipment to position the wafer and to orient the devices relative to the crystal in a specific manner. The secondary flat regions are used to identify the orientation and conductivity type of the crystal. The conductivity of the wafer could be either *P*-type or *N*-type and the crystal orientation, {100} or {111} (refer to Art 50.16 to know more about crystal orientation). If there is no secondary flat as shown in Fig. 67.7 (*a*), or in words the primary and the secondary flat are superimposed, the wafer is identified as *P*-type with {111}-crystal orientation. If the secondary flat is 45° with respect to the primary flat as shown in Fig. 67.7 (*b*), it is {111} *N*-type wafer. However, if the secondary flat is 90° with respect to the primary flat as shown in Fig. 67.7 (*c*), it is {100} *P*-type wafer and if the secondary flat is at 180° with respect to the primary flat as shown in Fig. 67.7 (*d*), it is {100} *N*-type wafer.

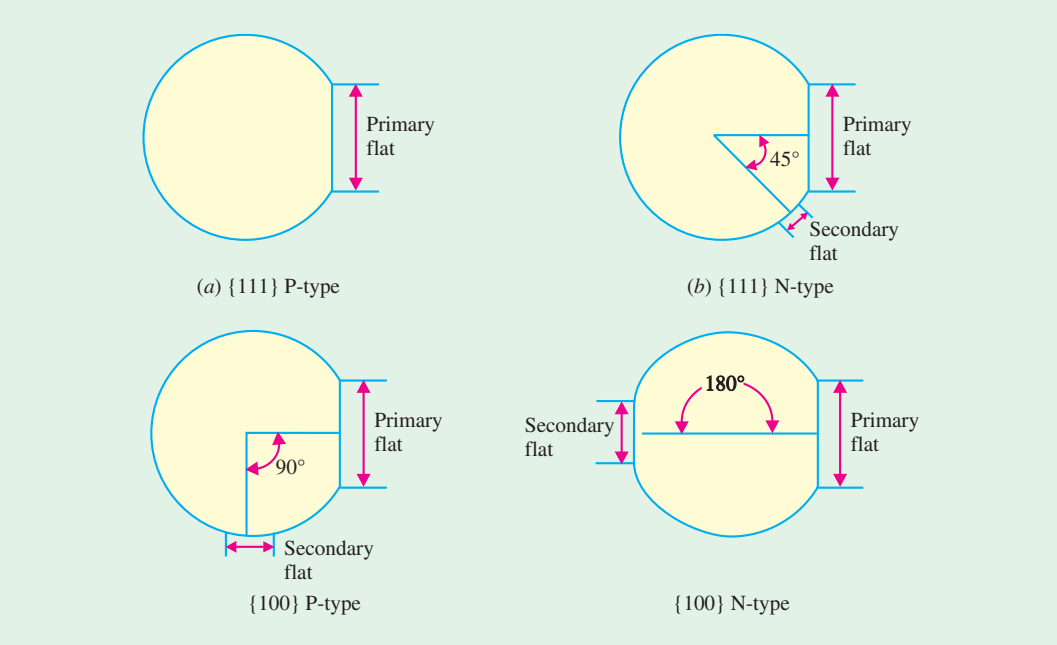


Fig. 67.7

The semiconductor industry uses {111} wafers for fabricating *ICs* with bipolar transistor technology and {100} wafers for metal-oxide semiconductor (MOS) circuits. The choice of wafer conductivity (*i.e.*, *P*-type or *N*-type) depends upon the actual process used for fabricating the *ICs*. Once the orientations are done, the ingot is sliced into wafers by a high-speed ***diamond saw.*** The wafer thickness varies from 0.4 to 1.0 mm.

After slicing, both sides of the wafer are lapped to produce typical flatness uniformity with in 2 μm. The lapped orientation usually leaves the surface and edges of the wafer, damaged and contaminated. These can be removed by a process called chemical etching. The next step is to polish the wafer surface to a mirror-like finish. Finally the wafers are cleaned, rinsed and dried for use in fabrication of *ICs*. It is interesting to note that the final wafer thickness is about one-third less than after the slicing.

67.17. Wafer Fabrication

Following is the category of the processes that are used in the fabrication of *ICs* :

(*i*) oxidation **(*ii*)** etching **(*iii*)** diffusion
(*iv*) ion implantation **(*v*)** photolithography **(*vi*)** epitaxy
(*vii*) metallization and interconnections.

We will study each process separately and apply some of these later to the formation of a diode bipolar transistor and metal oxide semiconductor field effect transistor. The basic fabrication process is called ***planar process,*** *i.e.*, a process in which the introduction of impurities and metallic interconnections is carried out from the top of the wafer. A major advantage of the planar process is that each fabrication step is applied to all identical circuits and each of the many wafers at the same time.

It is important to initially emphasize that the fabrication requires an extremely clean environment in addition to the precise control of temperature and humidity.

67.18. Oxidation

The process of oxidation consists of growing a thin film of silicon dioxide (SiO_2) on the surface of a silicon wafer. Silicon dioxide has several uses :

1. to serve as a mask against implant or diffusion of dopant into silicon,
2. to provide surface passivation,
3. to isolate one device from another,
4. to act as a component in MOS structures.

Fig. 67.8 shows oxide layer grown on the surface of silicon substrate. The commonly used silicon dopants, such as boron, phosphorus, arsenic, and antimony, have very low diffusion coefficients (*i.e.*, they diffuse with great difficulty) in silicon dioxide. Because of this reason, silicon dioxide is used as a shield against infiltration of these dopants. On the other hand, these dopants diffuse easily if the surface is silicon.

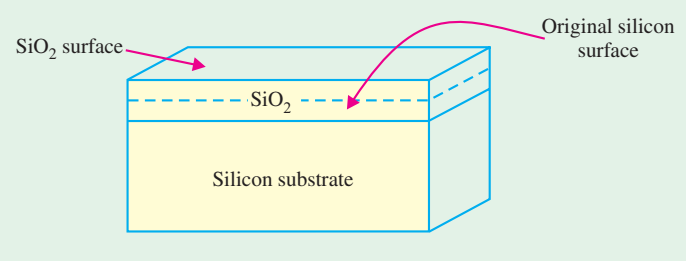


Fig. 67.8

Several techniques have been developed for forming oxide layers. Some of these are thermal oxidation, vapour phase technique [chemical vapour deposition (CVD)], and plasma oxidation. However, thermal oxidation is the more commonly used technique in *IC* processing.

Fig. 67.9 shows a thermal oxidation system. As seen, the oxidation is accomplished by placing the silicon wafers vertically into a quartz boat in a quartz tube. The quartz boat is slowly passed through a resistance heated furnace, in the presence of oxygen, operating at a temperature of about 1000°C. The oxidizing agent may be *dry* by using dry oxygen or be using a mixture of water vapour and oxygen. A computer controls the whole operation in the thermal oxidation system. The operation include regulating the gas flow sequence, automatic insertion and removal of wafers and the furnace temperature.

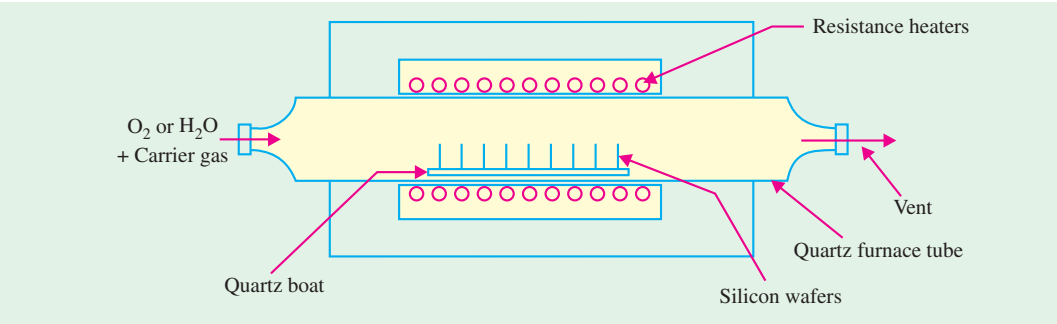


Fig. 67.9

It will be interesting to note that the oxide growth in the dry process is much ***slower*** but it produces an oxidized layer that has ***excellent*** electrical properties. For relatively thin oxides such as gate oxide in a MOSFET (typically 10 nm), dry oxidation is used. However, for thicker oxides (≥ 500 nm) such as field oxides in MOS integrated circuits and for bipolar devices, wet oxidation is used to provide both isolation and passivation.

Once the silicon dioxide layer has been formed on the surface of the wafer, it is selectively removed (etched) from those surfaces where impurities are to be introduced and kept as a shield, for the underlying silicon surface, where no dopants are to be allowed.

Oxide layers are relatively free from defects and provide stable and reliable electrical properties.

67.19. Etching

Etching is the process of selective removal of regions of a semiconductor, metal or silicon dioxide. There are two types of etching : ***wet*** and ***dry***. In wet etching, the wafers are immersed in a chemical solution at a predetermined temperature. In this process, the material to be etched is removed equally in all directions (*i.e.*, etching is isotropic). Because of this, some material is etched from the regions where it is to be left. This becomes a serious problem when dealing with small dimensions.

In dry (or plasma) etching, the wafers are immersed in gaseous plasma created by a radio-frequency electric field applied to a gas such as argon. The gas breaks down and becomes ionized. Electrons are initially released by field emission. These electrons gain kinetic energy from the field, collide with, and transfer energy to gas molecules, which result in generating ions and electrons. The newly generated electrons collide with other gas molecules and the avalanche process continues throughout the gas, forming plasma. The wafer to be etched is placed on an electrode and is subjected to the bombardment of its surface by gas ions. As a result, the transfer of momentum from the ions to the atoms removes atoms at or near the surface to be etched.

Dry etching also called reactive ion etching (RIE) is directional (or anisotropic). In other words, the material is removed only from those regions where it is required. Most modern processes use only dry etching to produce fine line patterns needed for VLSI integrated circuits.

67.20. Diffusion

This process consists of the introduction of impurities into selected regions of a wafer to form junctions. Diffusion occurs in two steps : the ***pre-deposition*** and the ***drive-in*** diffusion. In the pre-deposition step, a high concentration of dopant atoms is introduced at the silicon surface by a vapour that contains the dopant at a temperature of 1000°C. More recently, a more accurate method of pre-deposition known as ***ion implantation*** is used.

Pre-deposition tends to produce, a shallow but heavily doped layer, near the silicon surface. Drive-in is used to drive the impurity atoms deeper into the surface, without adding any more impurities. Fig. 67.10 shows the graph of doping profiles, (*i.e.*, impurity concentration versus depth into the substrate) during the pre-deposition and the drive-in steps of diffusion. The doping profiles indicate that the impurity concentration decreases monotonically from the surface of the substrate. The profiles of the dopant distribution is determined mainly by the temperature and diffusion time. Note that the impurity concentration drops from *OA* (during pre-deposition step) to *OB* at the surface of the substrate after the drive-in step. However the depth into the substrate of impurity has increased from *OC* to *OD* as required.

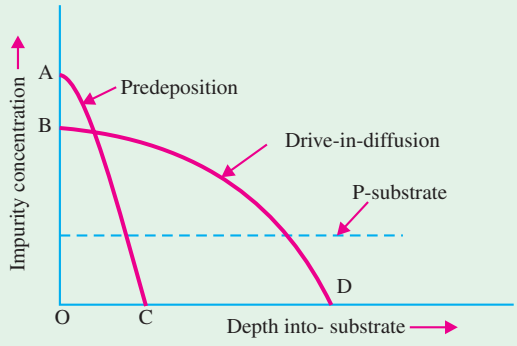


Fig. 67.10

Common dopants are boron for *P*-type layers and phosphorus, antimony and arsenic for *N*-type layers. However, diffusion is rarely performed using pure elements themselves. Rather, compounds of elements are used and impurities may be introduced from either solid, liquid, or gaseous substances.

Fig. 67.11 shows the equipment used in diffusion. The wafers are placed in a quartz boat within a quartz furnace tube. The furnace is heated by resistance heaters surrounding it. To introduce an impurity, phosphorus for example, phosphorus oxychloride ($POCl_3$) is placed in a container either inside the quartz tube in a region of relatively low temperature or in a container outside the furnace at a temperature that maintains its liquid form. For a *P*-type dopant, boron is used. The proper vapour pressure is maintained by a control of the temperature. Nitrogen and oxygen gas are made to pass over the container. These gases react with the silicon, forming a layer on the surface of the wafer that contains silicon, oxygen and phosphorus. At the high temperature of the furnace, phosphorus easily diffuses into the silicon.

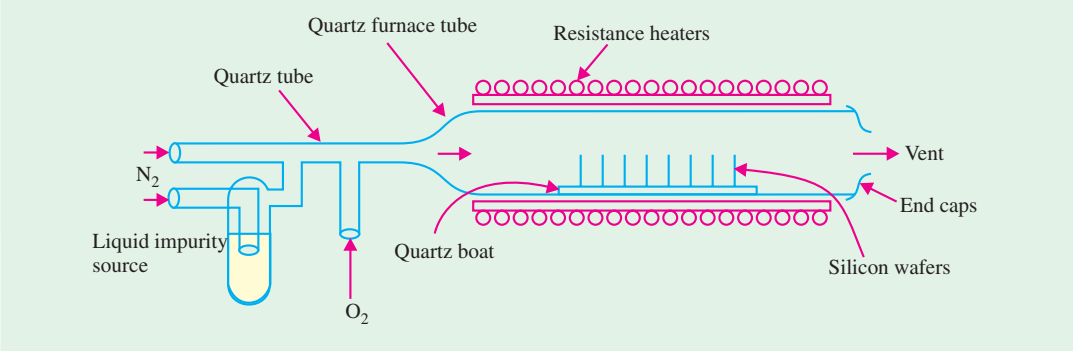


Fig. 67.11

In order that the dopant may be diffused deeper into silicon, the drive-in step follows. This is done at a higher temperature of about 1100°C inside a furnace similar to that used for pre-deposition, except that no dopant is introduced into the furnace. The higher temperature, causes the dopant atoms to move into silicon more quickly. Diffusion depth is controlled by the time and temperature of the drive-in process. By precise control of the time and temperature, accurate junction depths of fraction of a micron can be obtained. Fig. 67.12 shows the diffusion of dopant into silicon.

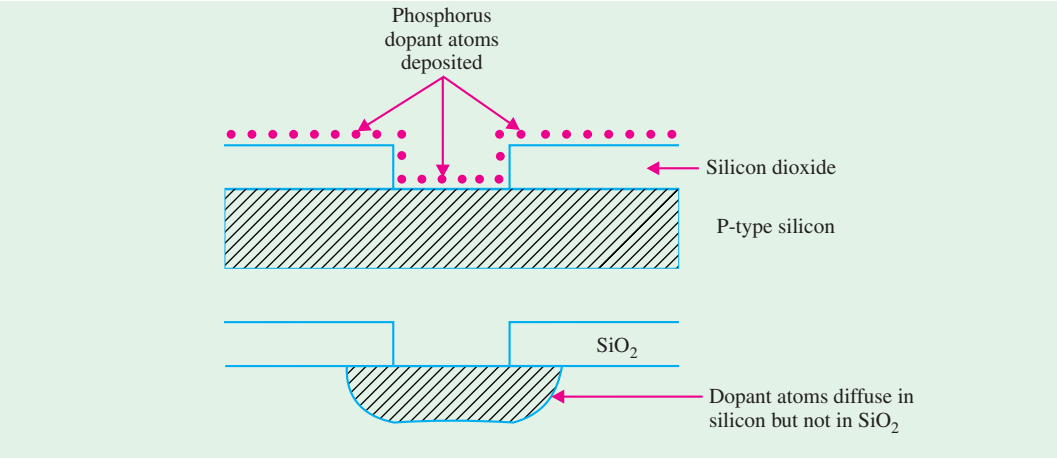


Fig. 67.12

67.21. Ion Implantation

This is a process of introducing dopants into selected areas of the surface of the wafer by bombarding the surface with high-energy ions of the particular dopant.

Fig. 67.13 shows a typical ion implantation equipment. To generate ions, such as those of phosphorus, an arc discharge is made to occur in a gas, such as phosphine (PH_3), that contains the dopant.

The ions are then accelerated in an electric field so that they acquire energy of about 20 keV and are passed through a strong magnetic field. The ions are further accelerated so that their energy reaches several hundred keV or MeV, whereupon they are focused on and strike the surface of the silicon wafer.

As is the case with diffusion, the ion beam is made to penetrate only into selected regions of the wafer by a process of masking (discussed later). On entering the wafer, the ions collide with silicon atoms and lose their energy. The depth of penetration of ions in ion implantation is about 0.1 to 1 μm. The higher the energy of ions and the smaller their mass, the greater is the depth of penetration.

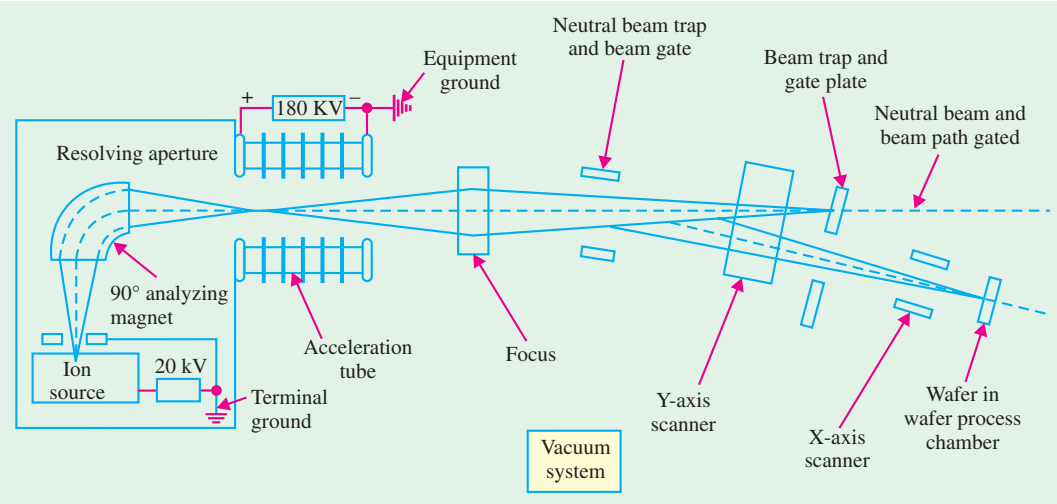


Fig. 67.13

Advantages of ion implantation over diffusion :

1. Doping levels can be precisely controlled since the incident ion beam can be accurately measured as an electric current.
2. The depth of the dopant can be easily regulated by control of the incident ion velocity. It is capable of very shallow penetrations.
3. Extreme purity of the dopant is guaranteed.
4. The doping uniformity across the surface can be accurately controlled.
5. Because the ions enter the solid as a directed beam, there is very little spread of the beam, thus the doping area can be clearly defined.
6. Since ion implantation is carried out at room temperature, wafers do not face temperature stress. In addition photo-resist can be used as mask for masking impurities, thus there is no need to grow thick masking oxides.

Disadvantages of ion implantation over diffusion :

1. The ion implantation may create considerable damage to the crystal structure because of the collisions of the high-energy ions with the silicon. Such damage results in inferior performance of *ICs* made by this process. If the damage is not extensive, the process of ***annealing*** restores the structure.
2. High initial investment and operational cost of the equipment (> US $ 1 million).
3. Uses very toxic gases for some of the dopants such as phosphorus and arsenic.

67.22. Photomask Generation

The whole process of *IC* fabrication consists of identifying selected regions of each circuit of the wafer surface into which identical dopant or metallic interconnections are made, while protecting other regions of the wafer surface. To carry out one of the many fabrication processes, a separate

mask is required for each operation whose function is to expose the selected regions and protect the others. There may be hundreds of identical dies (or *ICs*) on a wafer with each circuit containing hundreds of thousands or millions of devices. Identical steps are carried out simultaneously for each process. For each process, separate mask is needed.

The mask production starts with a drawing using a computer-assisted graphics system with all the information about the drawing stored in digital form. Commands from the computer are prepared that drive a pattern generator, which uses an electron beam to write the particular pattern, for one or several dies, on a glass plate covered with thin chromium film. When the glass plate is prepared, it is called ***reticle***. A mask usually refers to a glass plate that contains a pattern for the whole wafer. The reticle pattern is projected onto the wafer and a ***wafer stepper*** is used that reduces the reticle circuit onto the photo-resist covered wafer that steps across over the surface until the entire array of circuits is built up.

It may be noted that the use of a single mask for all the circuits on a wafer is not feasible for printing very small (< 1 μm) features because of alignment problems. However, the use of single mask is still in use for fabricating simple digital and analog circuits such as light emitting diodes (LEDs).

67.23. Photolithography

It is a process in which the geometrical pattern on the glass plate (called reticle) is transferred to the surface of the wafer. This is done to open identical windows so that the diffusion (or the ion implantation) process may take place in all identical regions of the same *IC* and for all *ICs* on the wafer. As an illustration we assume that the first reticle is used over an oxidized surface as shown in Fig. 67.14 (*a*).

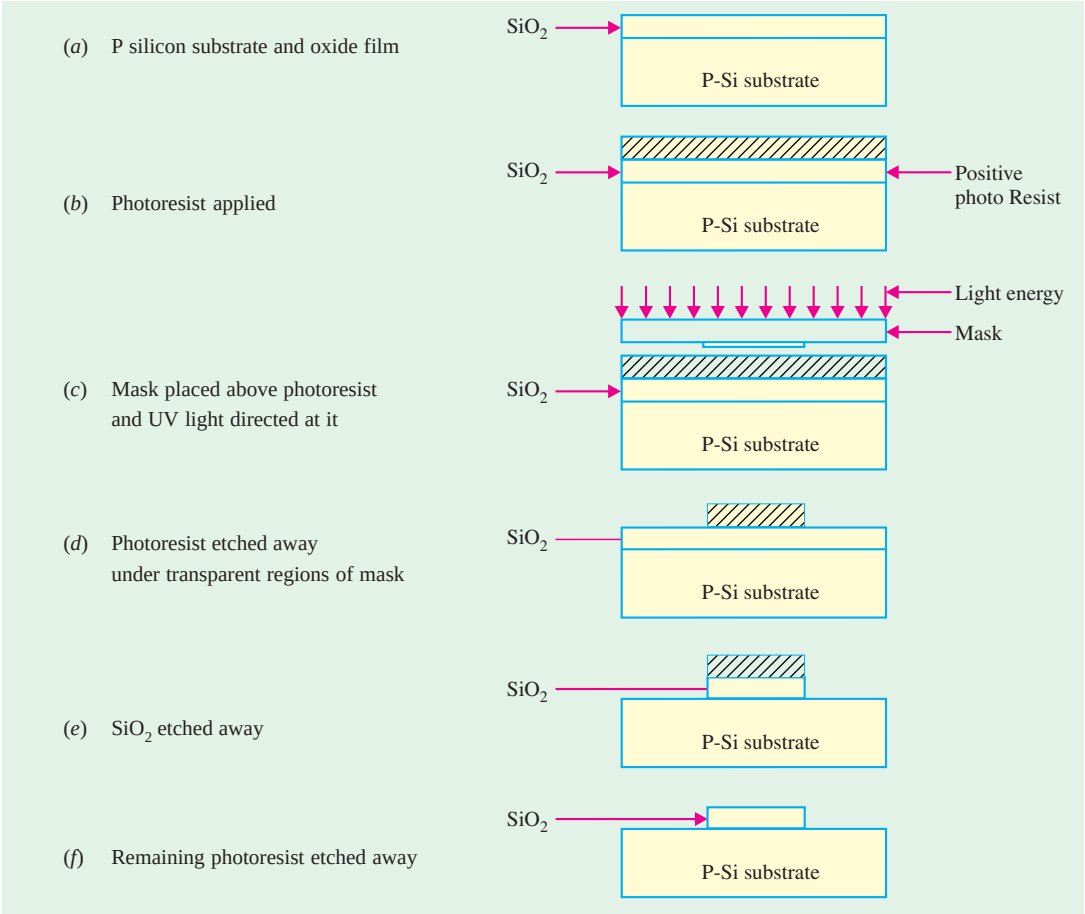
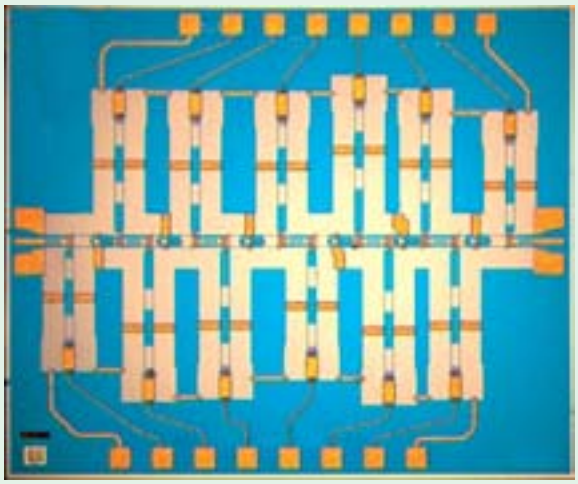


Fig. 67.14

To transfer the patterns, the wafer is coated with light-sensitive material called ***photoresist.*** By applying small amount (about 1 ml) of the photoresist to the wafer surface and spinning the wafer very rapidly, a uniform film of about 1 μm thick is formed over the oxidized surface of the wafer [refer to Fig. 67.14 (*b*)]. After this the following steps are taken to open a window on the surface of the wafer :

1. The wafer is baked at 100°C to solidify the photoresist on the wafer.
2. The glass plate is placed on the wafer and aligned by the computer control.
3. The glass plate is exposed to ultraviolet (UV) light with the transparent parts of the glass plate passing the light on to the wafer. The photoresist under the opaque regions of the glass plate is unaffected [refer to Fig. 67.14 (*c*)].
4. The exposed photoresist is chemically removed by dissolving it in an organic solvent and exposing the silicon dioxide underneath [refer to Fig. 67.14 (*d*)].
5. The exposed silicon dioxide is then etched away using hydrofluoric acid. The hydrofluoric acid dissolves silicon dioxide and not silicon. The regions under the opaque part of the glass plate are still covered by the silicon dioxide and the photoresist [refer to Fig. 67.14 (*e*)].
6. The photoresist under the opaque regions of the glass plate is removed using a proper solvent and the silicon dioxide is exposed [refer to Fig. 67.14 (*f*)].

All surfaces in Fig. 67.14 (*f*) are protected except those covered by silicon only in which diffusion or ion implantation is to take place. It may be noted that the surfaces covered by silicon dioxide do not permit any entry of dopants.



The photolithograph is used to add circuit elements to the wafer. The wafer is coated with layer of a chemical called photoresist.

The photoresist used in the explanation above is called a ***positive photoresist.*** Thus a positive photoresist is that which allows the windows to be opened wherever the UV light passes through the ***transparent*** parts of the mask. On the other hand a photoresist which remains on the surface, when exposed to UV light, and windows are opened under the ***opaque*** parts of the mask, is called a ***negative photoresist.*** The negative photoresist is limited to a resolution of 2 to 3 μm. On the other hand, the positive photoresist sacrifice adhesion and simplicity of development to achieve higher resolution.

The method of using UV light has a practical limit for transferring patterns on the silicon. It can be used for the patterns where the linewidths are above 1 to 2 μm. In order to transfer small patterns (*i.e.*, those with below 1 μm linewidth), very short wavelength radiation such as electron-beam or *X*-rays are used.

67.24. Epitaxy

Epitaxy or **Epitaxial growth** is the process of the ***controlled growth*** of a crystalline doped layer of silicon on a single crystal substrate. The process of diffusion and ion implantation, which

were earlier described, produce a layer at the surface that is of higher doping density than that which existed before the dopant was added. It is not possible by these methods to produce, at the surface a layer of lower concentration than exists there. This can however, be accomplished by the method of epitaxy. In the processes of diffusion and ion implantation, a dopant is driven into a substrate of doped silicon. In epitaxy, a layer of doped silicon is deposited on top of the surface of the substrate. Normally this single crystal layer has different type of doping from that of the substrate.

Epitaxy is used to deposit N or N^+ (*i.e.*, heavily doped *N*-type) silicon, which is impossible to accomplish by diffusion. It is also used in isolation between bipolar transistors where N^- (*i.e.*, lightly doped *N*-type) is deposited on *P*-type layer. It may also be used to improve the surface quality of an *N*-type substrate by depositing *N*-type material over it. A variety of methods are used to grow the epitaxial layer. These methods include vapour-phase epitaxy (VPE), liquid-phase epitaxy (LPE), and molecular beam epitaxy (MPE). The system for growing an epitaxial layer using vapour-phase epitaxy (VPE) is shown in Fig. 67.15.

In this system, silicon wafers are placed in a long boat-shaped crucible made of graphite. The boat is placed in a long cylindrical quartz tube, which has inlets and outlets for the gases. The tube is heated by induction using the heating coils wound around the tube.

All the chemicals that are introduced and that take part in the reactions are in the form of gases, hence the process is known as Chemical Vapour Deposition (CVD). The epitaxial layer is grown from the vapour phase onto the silicon, which is in the solid state. The thickness of the layer varies from 3 to 30 μm and the thickness of the layer and its doping content are controlled to an accuracy of less than 2 percent. The reactions are carried out at a temperature of approximately 1200°C. The high temperature is necessary so that the dopant atoms can acquire a sufficient amount of energy to allow them to move into the crystal to form covalent bonds and become extension of the single crystal. Because the layer is grown on the substrate, epitaxy is a growth technique where the crystal is formed without reaching the melting point of silicon.

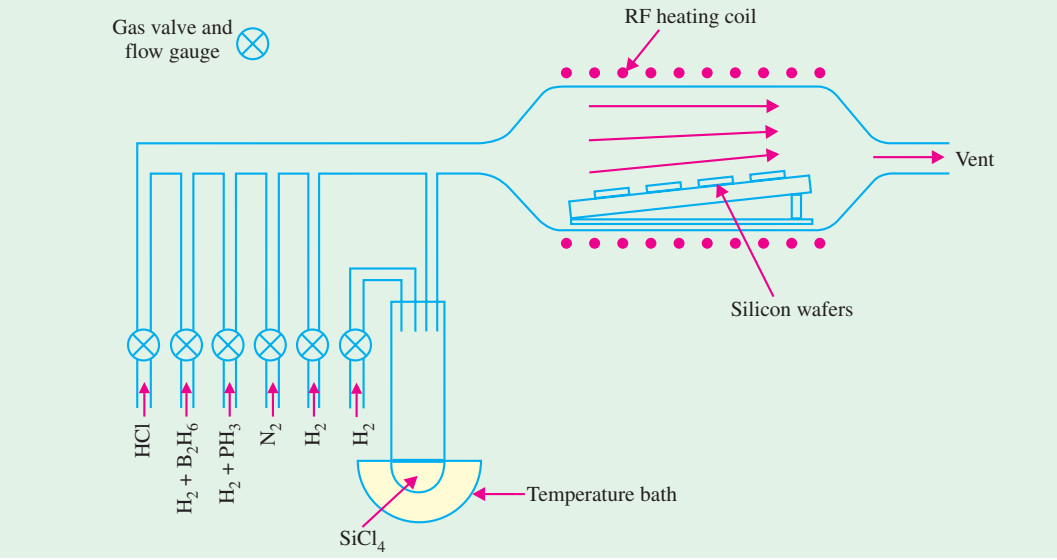


Fig. 67.15

67.25. Metallization and Interconnections

After all the fabrication steps of an *IC* are completed, it becomes necessary to provide metallic interconnections for the *IC* and for external connections to the *IC*. The requirement that must be met by the interconnections is that they have low resistance to minimize both the voltage drops on the lines as well as the capacitances between the lines so as to reduce delay times. The connections must

also make ***ohmic contacts*** to semiconductors in the devices such as *P* and *N* regions of a *PN* junction diode. An ohmic contact is one that exhibits a very low resistance, allowing currents to pass easily in both directions through the contact.

The high conductivity of aluminium makes it the metal of obvious choice, particularly in silicon-based devices. It also has the following advantages :

1. easy to evaporate
2. can be easily etched
3. not expensive,
4. adheres well to silicon dioxide.

There are variety of processes for depositing aluminium on silicon substrates but the following three are important from the subject point of view : **(1)** resistance heating, **(2)** electron beam heating and **(3)** sputtering.

Several cycles of photolithography etching and doping are performed producing multiple layers of circuit elements on the wafer.

Resistance heating : In this process, the source of the heated element and the silicon substrate are located in an evacuated chamber. The source is a small piece of aluminium attached to a coil of tungsten, which serves as a heater [refer to Fig. 67.16 (*a*)]. The heated element with a high melting point remains solid while the aluminium is vaporized. The aluminium atoms travel to the substrate where they condense, depositing an aluminium layer on the surface of the silicon. A photolithographic masking and etching method is used to remove the metal from the regions where it is not wanted. A typical interconnection between two diffused layers is as shown in Fig. 67.16 (*b*).

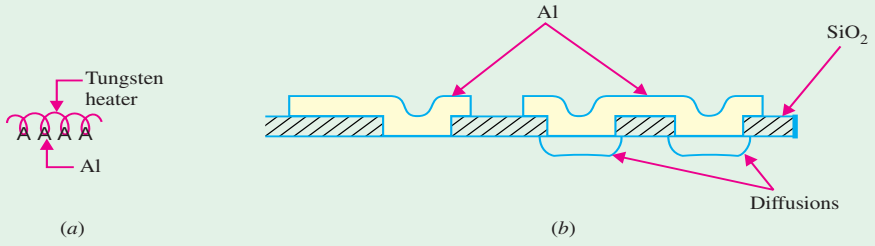


Fig. 67.16

In another method, the evaporation source kept in a boron nitride crucible is heated by radio frequency induction as shown in Fig. 67.17 (*a*). High deposition rates are possible through this process. However, the crucible may contaminate the metal.

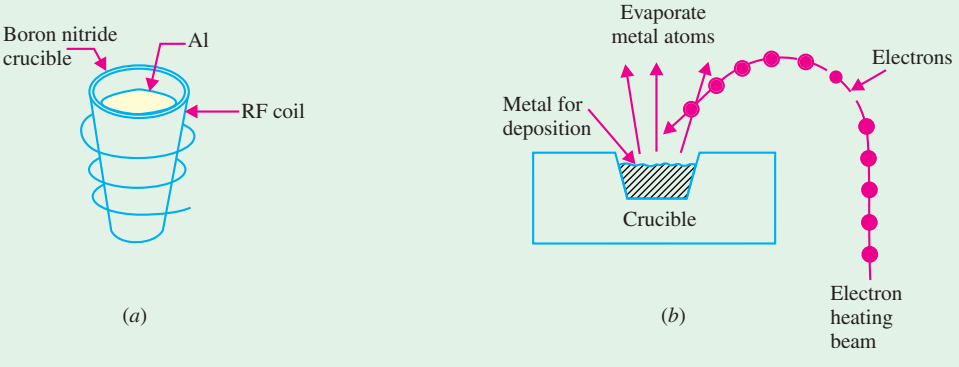


Fig. 67.17

Electron-beam heating : In this process, aluminium in a crucible is placed into a vacuum chamber together with the substrate. The aluminium is subjected to a high intensity electron beam formed by an electron gun, which vaporizes the aluminium as shown in Fig. 67.17 (*b*). This causes the aluminium to travels to the wafer. By the use of mask and photolithography, the aluminium is deposited on the identified regions on the wafer surface.

Sputtering : In this process, the material to be deposited is placed in a container maintained at low pressure in the vicinity of the substrate. The material to be deposited is labelled the cathode or the target, while the anode is the substrate. A DC or a radio-frequency high voltage is applied between anode and cathode. This high voltage ionizes the inert gas in the chamber. The ions are accelerated to the cathode (in this operation the anode is usually grounded) where, by impact with the aluminium target, atoms of aluminium are vaporized. A gas of aluminium atoms is generated and deposited on the surface of the wafer.

Following the deposition of aluminium, the silicon wafers are placed in a furnace to solidify the connections so that low resistance metallic contacts are made.

The interconnections between the elements of an *IC* are made by aluminium lines having a thickness of about 0.5 μm. These are laid on top of the silicon dioxide layer, which covers the surface of the wafer. By using photolithography, openings are made in silicon dioxide so that the aluminium layer is connected to the silicon or to the ohmic contact on the silicon. In very complicated integrated circuits, it is necessary to have two or three vertically stacked layers of interconnections separated by silicon dioxide layers. The interconnecting lines terminate at aluminium pads (called bonding pads) from which connections to the outside are made.

67.26. Testing, Bonding and Packaging

The individual *IC* chip must be connected properly to outside leads and packaged in a way that is convenient for use in a larger circuit or a system. Since the devices are handled individually once they are separated from the wafer, bonding and packaging are expensive processes.

Testing – After the wafer of monolithic circuits has been processed and the final metallization pattern defined, it is placed in a holder under a microscope and is aligned for testing by a machine called ***multiple-point probe.*** The probe contacts the various pads on an individual circuit, and a series of tests are made to verify the electrical properties of the device in a very short time. After all the circuits are tested, the wafer is removed from the testing machine, sawed between the circuits, and broken apart. Then each die that passed the test is picked up and placed in the package.

Bonding – It consists of two steps. In the first step the back of the die is mechanically attached to an appropriate mount medium such as ceramic substrate, multi-layer-ceramic package or metal lead frame. The two common die bonding methods are ***hard solders*** and ***polymers.*** In the second step, the bond pads on the circuit side of the die are connected by wires to the package as shown in Fig. 67.18. The three common schemes of interconnection to the chip bond pads are ***(i) wire bonding, (ii) tape-automated bonding*** (*TAB*), and ***(iii) flip-chip solder bonding.*** Wire bonding is further split into two different processes : ***thermosonic*** and ***thermocompression.*** The further detail of these processes is beyond the scope of this book.

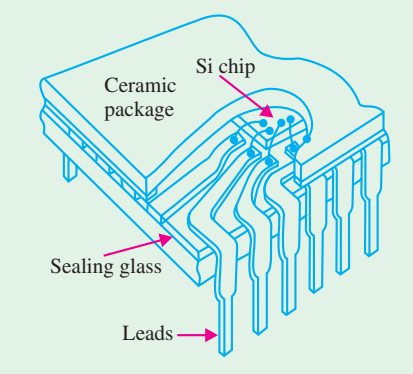


Fig. 67.18

Packaging – The final step in *IC* fabrication is packaging the device in a suitable medium that can protect it from environment of its intended application. In most cases this means the surface of the device must be isolated from the moisture and contaminants and the bonds and other elements must be protected from corrosion and mechanical shocks. The modern *ICs* are mounted in pack-

ages with many output leads. In one version, chip is mounted on a stamped metal lead frame and wire bonding is done between the chip and the leads. The package is formed by applying a ceramic or plastic case and trimming away the unwanted parts of the lead frame.

Fig. 67.19 shows various types of the packaging of *ICs* used these days. As seen from this figure, the packages can be broadly classified into the following two categories :

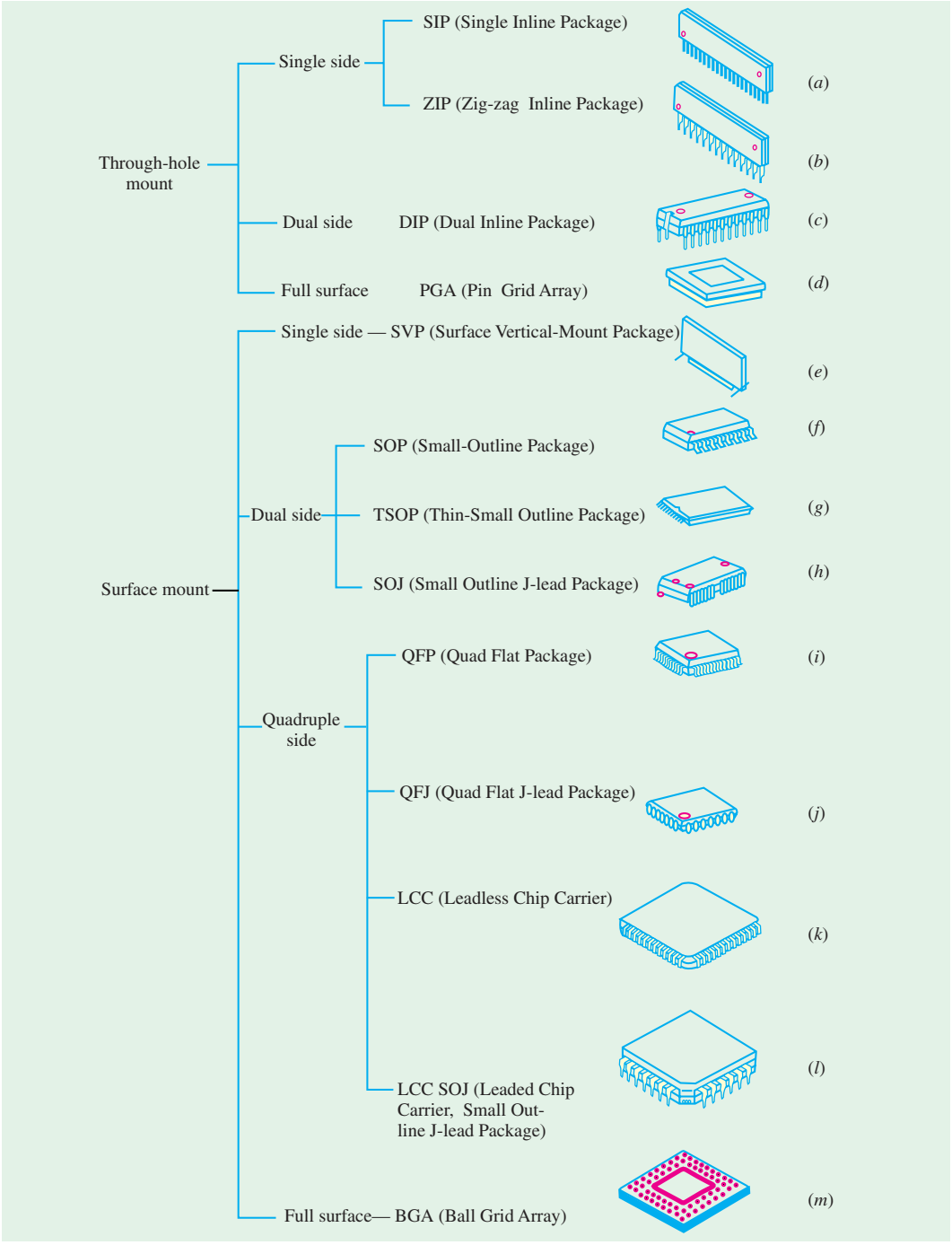


Fig. 67.19

1. ***through-hole mount*** that involve inserting the package pins through holes on the printed circuit board (PCB) before soldering [Fig. 67.19 (*a*) through (*d*)].
2. ***surface mount type*** where the leads do not pass through holes in the PCB. Instead, surface-mounted package leads are aligned to electrical contacts on the PCB, and are connected simultaneously by solder reflow [Fig. 67.19 (*e*) through (*m*)]. As refer to the picture shown in Fig 67.20.

Most packages can be made using ceramic or plastic. The *ICs* are hermetically sealed for protection from the environment. The pins can be on one side (single inline or zigzag pattern of leads), two sides (dual inline package or DIP), or four sides of the package (quad package). Most advanced packages have leads distributed over a large portion of the surface of the package as in through-hole pin grid arrays (PGAs) or surface-mounted ball grid arrays (BGAs).

67.27. Semiconductor Devices and Integrated Circuit Formation

There are literally thousands of different semiconductor device structures. They have been developed to achieve specific performances, either as discrete components or in *ICs*. Accordingly there are many different structures. However, there are basic structures required for each of the major device and circuit types.

Fig. 67.20

1. ***Resistors :*** Most of the resistors in *ICs* are formed by the same processes that are used to form devices (*i.e.*, a sequence of oxidation, masking and doping operation). Fig. 67.21 (*a*) shows a resistor made of a *P*-type region diffused into an *N*-type epitaxial layer. Notice the metallic contacts made at the two ends of the epitaxial layer. The section of the resistor, as dictated by the diffusion, is very nearly rectangular in shape, as shown in Fig. 67.21 (*b*). The value of a resistor (in ohms) is given by :

$$R = \rho . l/a \quad \text{or} \quad \rho.l/w.d$$

where ρ is the resistivity of the layer in ohm-cm, l is the length of the resistive region, and a is the cross-sectional area of the resistive region. The value of a is equals to $w.d$. where w is the width and d is the depth of the resistive region.

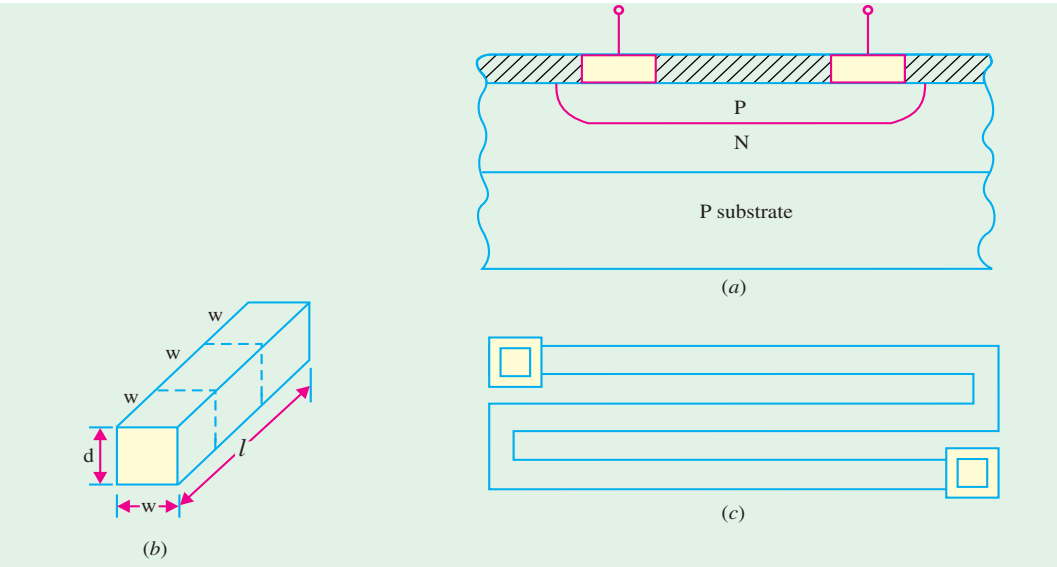


Fig. 67.21

Resistance in monolithic circuits are defined by the term called ***sheet resistance.*** The sheet resistance is the resistance of a square region having $w = l$ and has units of ohms per square. Assuming a sheet resistance of 100 to 200 ohms per square, practical resistors may have values ranging from 100 to several kilohms. Higher resistance values are obtained by using a meander pattern as shown in Fig. 67.21 (*c*). The major problem with the resistors of high values is that they tend to occupy a large area on the chip. For example, a resistor of 50 kΩ uses up an area of the wafer that may be occupied by hundreds of the transistors. Ion-implantation instead of diffusion can be used to make resistors with precise values of resistance.

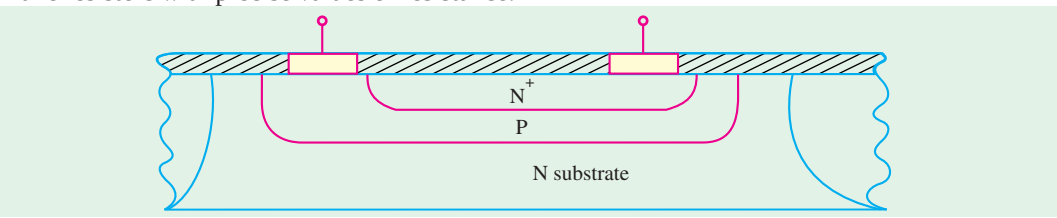


Fig. 67.22

2. *Capacitors :* One type of capacitor in monolithic circuits is made by using the capacitance formed between the *P* and *N* regions of a reverse-biased diode. Such a capacitor is shown in Fig. 67.22. These capacitors are formed by using the same diffusion processes that are used to form devices. Bipolar transistors are made of three regions in which either of the two *PN* junctions may be used as capacitors whereby the breakdown voltage of the capacitor may vary considerably from one to the other. The disadvantage of the junction capacitors is the dependence of the capacitance on the voltage applied to the junction. Capacitors that are voltage-independent can be formed from metal insulator N^+ (*i.e.*, heavily-doped) semiconductor layers as used in MOS structures.

In dense circuits, an oxide/nitride/oxide dielectric sandwich is used. The combination film has a lower dielectric constant, allowing a capacitor area smaller than a conventional silicon dioxide capacitor.

Capacitors can also be fabricated by creating a trench etched vertically into the wafer surface (refer to Fig. 67.23). The trenches are etched either isotropically with wet etching or anisotropically with dry etching techniques. The trench side walls are oxidised and the centre of the trench is filled with deposited polysilicon. The final structure is "wired" from the surface, with the silicon and polysilicon serving as two electrodes and silicon dioxide as a dielectric material.

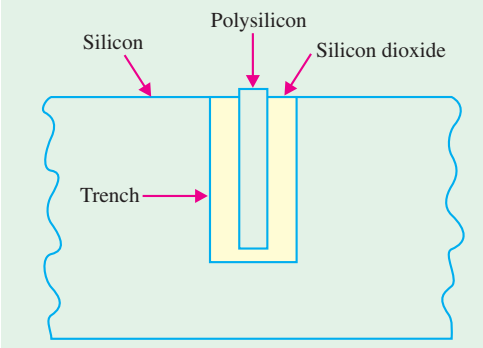


Fig. 67.23

The trenched capacitors are useful when preservation of wafer surface is main criteria. Another alternative to conserve wafer surface area is to build stacked capacitors on the wafer surface. This effort has been driven by the need for small high dielectric capacitors for dynamic random access memory (DRAM) circuits.

3. *Diodes :* In integrated circuits, where all the interconnections and device terminals are made at the surface, a diode is formed in the following two ways :

(*a*) In bipolar circuits from a bipolar transistor by placing a ***short-circuit*** between two of the three terminals of the transistor (*i.e.*, collector to base or emitter to base). Thus there are emitter-base diodes and base-collector diodes.

(*b*) In MOS circuits, most of the diodes are formed with the source-drain doping step.

However, in order to make a discrete *PN* junction diode, we will discuss the various steps involved in the fabrication.

The starting material is a heavily doped *N*-type (N^+) substrate about 150 μm thick. A layer of *N*-type silicon (1 to 5 μm) is grown on the substrate by epitaxy as shown in Fig. 67.24 (*a*). Then a layer of silicon dioxide (SiO_2) is deposited by oxidation as shown in Fig. 67.24 (*b*). Next, the surface is coated with positive photoresist as shown in Fig. 67.24 (*c*). Then a mask is placed on the surface of silicon, aligned and exposed to ultraviolet light (UV) as shown in Fig. 67.24 (*d*). Next, mask is removed, resist is removed and silicon dioxide layer under the exposed resist is etched as shown in Fig. 67.24 (*e*). Then boron is diffused to form P-type region a shown in Fig. 67.24 (*f*). Note that boron diffuses easily in silicon but not in silicon dioxide. Next, a thin aluminium film is deposited over the surface as shown in Fig. 67.24 (*g*). Then the metallized area is covered with resist another mask is used to identify areas where metal is to be preserved. Wafer surface is etched to remove unwanted metal. Resist is then dissolved and we get a structure as shown in Fig. 67.24 (*h*). Finally, contact metal is deposited on the back surface and ohmic contacts are made by heat treatment.

4. *Bipolar Transistor* : Let us consider the fabrication of an NPN bipolar junction transistor (BJT) on a silicon wafer. While our discussion will be focussed on the BJT, it is understood that the surface of the whole wafer is being processed.

The starting material is a lightly doped *P*-type wafer. We will consider a small area on this wafer where we will form a BJT. The base on which the transistor is made is known as the substrate. The function of the substrate is to act as a mechanical support for the device. The reason for the use of a *P*-type substrate for the NPN transistor will be clarified when the term isolation is discussed. The substrate has a resistivity of 3-10 Ω cm with a thickness between 500 and 700 μm for wafers having diameters over 100 mm.

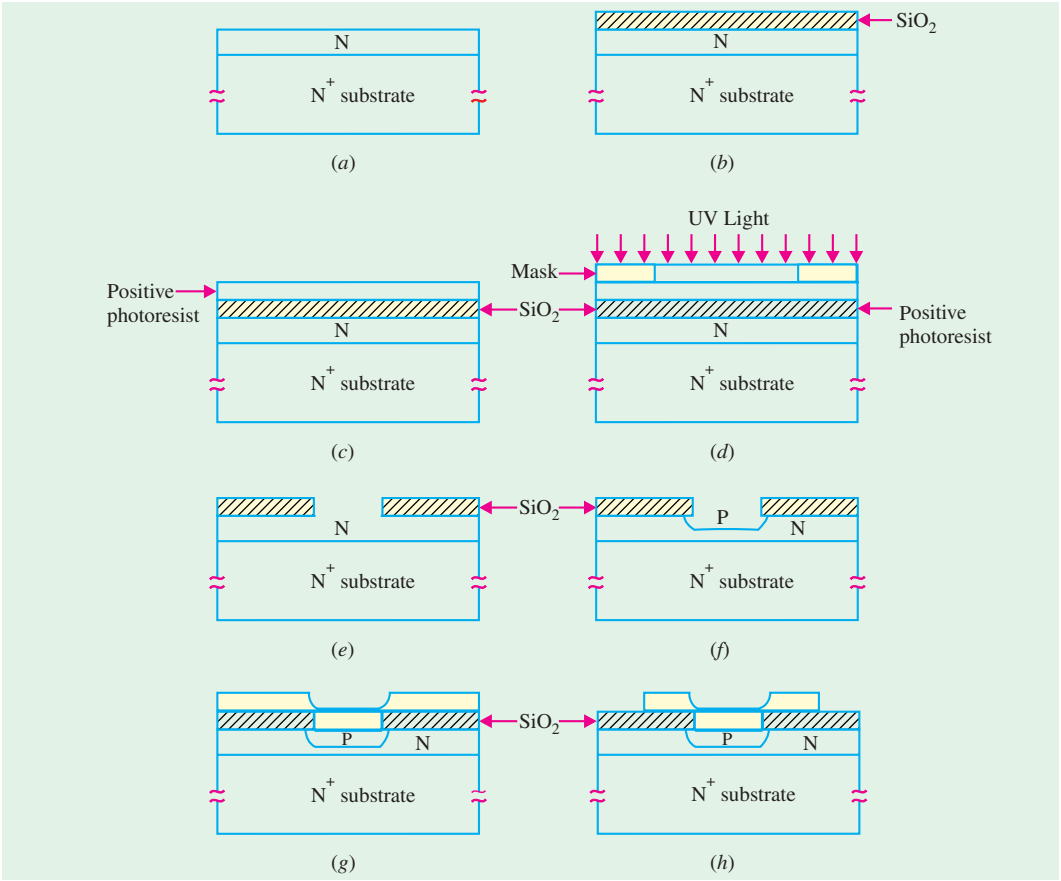


Fig. 67.24

Fig. 67.25 shows the fabrication steps up to, and including the metal contacts to the three regions (*i.e.*, emitter, base and collector).

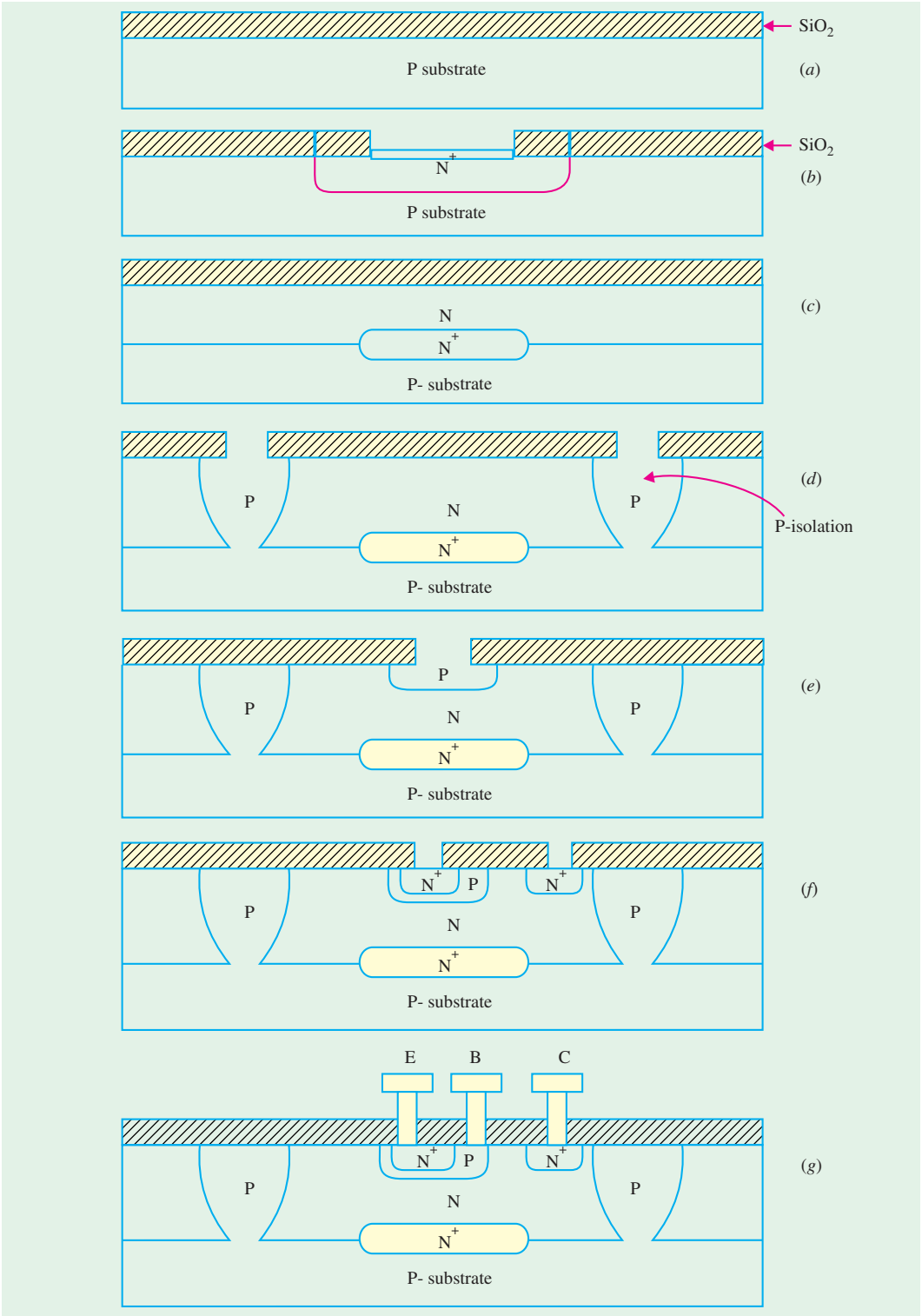


Fig. 67.25

First a layer of silicon dioxide (SiO_2), about 0.5 μm thick, is deposited on the surface of the substrate by thermal oxidation as shown in Fig. 67.25 (*a*). Using the ***first mask*** and the photolithographic process, windows are opened in the oxide for the *buried layer*. The N^+ (*i.e.*, heavily doped *N*-type) buried layer is diffused to a depth of about 3 μm as shown in Fig. 67.25 (*b*). This layer serves to collect the carriers that have crossed the base on their way to the collector terminal. It serves as a sub-collector and is used to reduce the collector ohmic-resistance. After the buried layer is diffused, the wafer is stripped of all oxide to permit the next deposition. It is to be noted that during the subsequent high-temperature processes, the buried layer tends to diffuse out.

The next operation is the deposition of a phosphorus-doped *N*-type ***epitaxial layer*** on the whole wafer. This layer has a resistivity of 0.1 to 1 Ω cm. The thickness of this layer is 0.5 to 5 μm for high-speed digital circuit applications and 10-20 μm for linear analog circuits. A layer of silicon dioxide (SiO_2) about 0.5 to 1 μm thick is grown thermally on the surface of the epitaxial layer as shown in Fig. 67.25 (*c*).

Since the collector of NPN transistor is *N*-type, and so are the collectors of the adjacent transistors, there is an obvious need to isolate the collectors from each other. The ***second mask*** is used to etch windows for this isolation regions, which are formed by the subsequent diffusion of boron extending from the surface down to the substrate as shown Fig. 67.25 (*d*). An *N*-type epitaxial layer separates the isolation regions, thus serving as the tub in which each transistor is formed. The diffusion of the isolation region is followed by oxidation of the wafer surface.

The ***third mask*** is used to open a window for the *P*-type base of the transistor, *P*-type diffusion or ion implantation is driven to form the base to a depth of about 2-3 μm as shown in Fig. 67.25 (*e*). This is followed by the deposition of an oxide layer. The ***fourth mask*** is used to open windows in the oxide for the N^+ emitter and the collector contacts. The phosphorus or arsenic diffusion is driven to a depth of about 2 μm as shown in Fig. 67.25 (*f*). The need for N^+ collector is to form a good ohmic contact. The ohmic contact permits easy current flow in both directions. To form a good ohmic contact to an *N* material, an N^+ region is needed between the metal on the top and the *N* region. Following the N^+ diffusion, an oxidation layer is formed over the entire wafer surface.

The ***fifth mask*** is used to open windows for the formation of metallic contacts to the bipolar transistor terminals. Then an aluminium film 0.5 and 1 μm thick is deposited, by evaporation or sputtering, on the top surface of the *IC* wafer. Assuming that the complete circuits are to be formed on the surface of the wafer, the ***sixth mask*** is used to define the interconnection pattern in the circuits. These interconnections are etched into the metal that has been deposited on the surface, as shown in Fig. 67.25 (*g*).

In order to protect the surface of the wafer from moisture and chemical contamination, a silicon nitride (Si_3N_4), called a ***passivation layer,*** is deposited on the surface. Contacts to the integrated circuits are made on pads that are located on the periphery of the *IC* chip. Since the *IC* chip will be bonded to an *IC* package, connections are to be made from the package leads to the bonding pads on the *IC* chip.

The ***seventh*** mask is used to define the bonding holes over the aluminium pads for external connections. Following the seven masks, the circuits are tested by a computer-controlled system and all faulty chips are identified and marked. The wafer is then sawed into chips, which are bonded on *IC* packages. Gold wires about 25 μm in diameter are used to connect the package leads to the bonding pads on the chip.

Fig. 67.26 shows an additional detail on the buried layer. It indicates the path taken by the carriers on their way from the emitter to the base and to the collector. This path is considerably longer than the path in the discrete BJT shown in Fig. 67.26 (*a*). Because of this the collector series resistance, labelled the ***parasitic resistance,*** is quite large and is of the order of hundreds of ohms. To reduce this resistance, we have placed the low resistivity buried layer in Fig. 67.26 (*b*) into the path of

the carriers which acts as a subcollector. The use of the buried layer reduces the collector resistance by as much as a factor of 20. The result of this is to improve gain-bandwidth product of the transistor by the same factor.

5. *MOSFET :* Let us consider the fabrication of Enhancement mode *N*-channel metal oxide semiconductor field-effect transistor. The starting material is a lightly doped *P*-type silicon substrate having a resistivity of about 5 Ω cm. The doping density is determined by the drain-substrate breakdown voltage of 20-30 V. A thin (about 20 nm) layer of silicon dioxide is formed over the substrate to provide stress relief to the wafer. Next a thin (about 20 nm) layer of silicon nitride (Si_3N_4) is deposited by the chemical vapour deposition (CVD) process on top of the silicon dioxide. The silicon dioxide permits selective oxidation so that a thick oxide (about 500 nm) can be formed in the field region. These operations result in Fig. 67.27 (*a*).

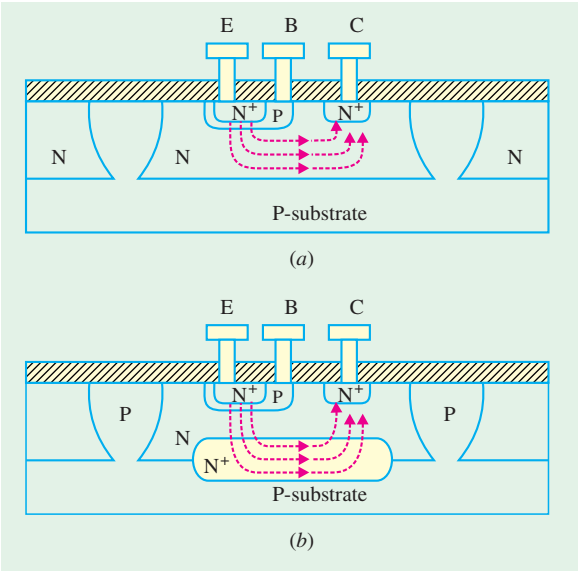


Fig. 67.26

The ***first mask*** defines the field-effect transistor areas, so that the silicon dioxide and the silicon nitride are chemically etched out except where the transistor is formed.

The next step is to diffuse (or ion-implant) boron in the field-regions to form P^+ (*i.e.* heavily doped *P*-type) islands in the substrate. The function of P^+ islands is to help increase the threshold voltage, V_T and prevent the formation of ***"parasitic" transistors*** (or electrical cross talk) between adjacent devices on the wafer. This is followed by the formation of a field oxide layer (about 500 nm thick) over the P^+ implanted region as shown in Fig. 67.27 (*b*). The field oxide layer also helps to increase V_T.

The remaining silicon nitride and silicon dioxide are etched away and an ultra thin (about 5 to 10 nm) layer of SiO_2 is grown over the transistor area (not above the field oxide). This forms the gate-oxide of the transistor. Refer to Fig. 67.27 (*c*). Next, a layer of heavily doped (typically N^+) polysilicon is deposited over the entire wafer surface. This is shown in Fig. 67.27 (*d*).

The ***second*** mask defines the gate region, whereupon the polysilicon is etched away except over the gate as shown in Fig. 67.27 (*e*). The heavily doped polysilicon region above the gate behaves electrically like a metal electrode.

By ion-implantation and using the polysilicon gate and the field oxide, as the mask, the source and drain N^+ regions are formed as shown in Fig. 67.27 (*e*). The N^+ layers literally diffuse a sufficient distance to ensure proper alignment so that the channel length is well defined. The dopants do not penetrate the field oxide. A thin layer of silicon dioxide is then grown, by the CVD process over the wafer.

The ***third mask*** is used to open windows for the metal contacts to the transistor regions as shown in Fig. 67.27 (*f*). The thin layer of silicon dioxide is etched away and aluminium is deposited over the surface of the wafer by evaporation or sputtering. The ***fourth mask*** defines the interconnection pattern that is etched in the aluminium, as shown in Fig. 67.27 (*g*). This is followed by the deposition of a protective passivation layer of phosphosilicate glass (called *P*-glass) over the entire surface of the wafer.

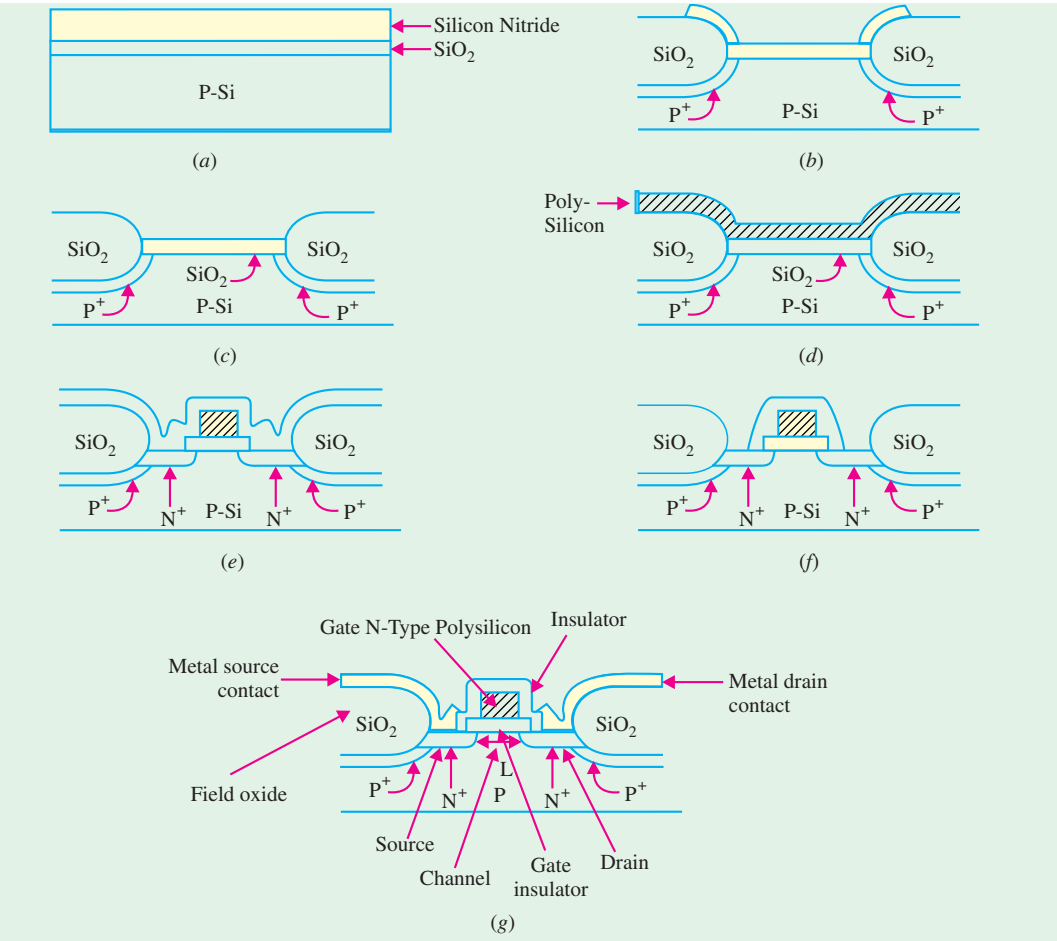


Fig. 67.27

Just as with the BJT, the ***fifth mask*** is used to open windows, so that bonding wires can be connected to the pads on the *IC* chip.

67.28. Comparison of ICs based on MOS and Bipolar Transistor Technology

1. The *ICs* based on MOS are less costly to fabricate as compared to those using bipolar transistor. The reason for this is that MOS devices are self-isolating. Bipolar transistors require tubs to isolate devices from each other on one integrated circuit. Isolation in MOS devices is provided by heavy doping and a thick oxide in the regions between adjacent devices.

2. MOS circuits consume less DC power as compared to bipolar transistor circuits.

3. The MOS transistor has lower value of transconductance (g_m) as compared to the bipolar transistor. This feature makes the bipolar transistor *ICs* superior to MOS circuits for analog circuit applications.

4. For the same channel length and the base width, the limiting cut-off frequency of the MOS transistor is better than a bipolar transistor. Therefore the MOS transistor has a higher bandwidth than the bipolar transistor.

5. The packing density of MOS *ICs* is at least 10 times more than that for bipolar *ICs*. Also, a MOS resistor occupies less than 1% of the area of a conventional diffused resistor. This high packing density makes MOS *ICs* especially suited for LSI, VLSI and ULSI circuits.

The main disadvantage of MOS *ICs* is their slower speed as compared to bipolar *ICs*. Hence they do not compete with bipolar *ICs* in ultrahigh-speed applications.

However, due to their ***(i)*** low cost, ***(ii)*** low power consumption and ***(iii)*** high packing density, MOS *ICs* are widely produced by semiconductor manufacturing industry. The MOS *ICs* are available as calculator chips, memory chips, microprocessors (μP), single-chip computers etc.

67.29. Popular Applications of ICs

There are plenty of electronic products in the market, which used integrated circuits extensively. One of the widely accepted applications is the digital watch, which can display hours, minutes, seconds, day and month. Another popular application is electronic calculator which can perform various functions like addition, subtraction, multiplication and division. There are also advanced scientific calculators that are programmable and can display the graphs.

Modern electronic products such as pocket PC, personal digital assistant (PDA), MP3 players, digital cameras, digital camcorders, mobile phones, digital dictionaries and digital translators, CD (compact disk) players, DVD (digital versatile disk) players etc. also make use of *ICs* extensively. With a Pocket PC, you can read and send e-mail, edit Word, Excel and Outlook files, listen to digital music, read electronic books (eBooks), track your finances, and browse the web. The digital camera shown in Fig. 67.28 can take pictures and store on the floppy diskette or memory stick. A personal digital assistant (PDA) as shown in Fig. 67.29 is a handheld computer which allows the user to organise calendar, contacts or tasks. These little electronic wonders might put office secretary out of a job.

Electronic games have evolved from microelectronics and computer knowhow. Video games that have to be hooked up to home TV have become very popular. Hand held PCs and mobile phones also come with games that require no TV hook-up.

Fig. 67.28
(courtesy Sony Corporation, Japan)

Fig. 67.29
(courtesy : 3Com, USA)

OBJECTIVE TESTS – 67

1. First integrated circuit chip was developed by
(*a*) C.V. Raman
(*b*) W.H. Brattain
(*c*) J.S. Kilby
(*d*) Robert Noyce.

2. An integrated electronic circuit is
(*a*) a complicated circuit
(*b*) an integrating device
(*c*) much costlier than a single transistor
(*d*) fabricated on a tiny silicon chip.

3. Most important advantage of an IC is its
(*a*) easy replacement in case of circuit failure
(*b*) extremely high reliability
(*c*) reduced cost
(*d*) low power consumption.

4. In monolithic ICs, all components are fabricated by ..... process.
(*a*) evaporation
(*b*) sputtering
(*c*) diffusion
(*d*) oxidisation.

5. Monolithic ICs are fabricated within a
(*a*) soft stone
(*b*) single stone
(*c*) silicon layer
(*d*) ceramic base.

6. As compared to monolithic ICs, film ICs have the advantage of
(*a*) better high-frequency response
(*b*) much reduced cost
(*c*) smaller size
(*d*) less flexibility in circuit design.

7. Monolithic technique is ideally suited for fabricating ..... ICs.
(*a*) thin-film
(*b*) digital
(*c*) linear
(*d*) thick-film

8. In the context of IC fabrication, metallisation means
(*a*) connecting metallic wires
(*b*) forming interconnecting conduction pattern and bonding pads
(*c*) depositing SiO_2 layer
(*d*) covering with a metallic cap.

9. Monolithic transistors are formed in the epitaxial *N*-layer
(*a*) in one operation
(*b*) by evaporation process
(*c*) by successive impurity diffusions
(*d*) by oxidisation.

10. The major component of a MOS IC is a/an
(*a*) FET (*b*) MOSFET
(*c*) BJT (*d*) SCR.

11. Processing of MOS ICs is less expensive than bipolar ICs primarily because they
(*a*) use cheaper components
(*b*) need no component isolation
(*c*) require much less diffusion steps
(*d*) have very high packing density.

12. In an integrated circuit, the SiO_2 layer provides
(*a*) electrical connection to the external circuit
(*b*) physical strength
(*c*) isolation
(*d*) conducting path.

13. The foundation on which an IC is built is called an
(*a*) insulator (*b*) base
(*c*) wafer (*d*) plate

14. Monolithic IC construction uses
(*a*) discrete components
(*b*) high-value resistors
(*c*) connecting wires
(*d*) extensive number of components

ANSWERS

1. (*c*) **2.** (*d*) **3.** (*b*) **4.** (*c*) **5.** (*c*) **6.** (*a*) **7.** (*b*) **8.** (*b*) **9.** (*c*) **10.** (*b*) **11.** (*c*) **12.** (*c*) **13.** (*c*) **14.** (*d*)

ROUGH WORK

GO To FIRST